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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,386	04/23/2001	Yoshihisa Matsubara	NEKA 18.612	2510

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EXAMINER	
VINH, LAN	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,386	MATSUBARA ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-11, 13-18* is/are pending in the application.

4a) Of the above claim(s) *4-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 13-16,18* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/840386* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action (mailed on 3/10/2005), presented on the response filed on 6/9/2005, is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 13, 14, 15, 16, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyawaki et al (US 5,952,694).

Miyawaki discloses a method for manufacturing a semiconductor device. This method comprises the steps of:

forming a first N-type region 14 and P-type region on a substrate (col 8, lines 63-64), forming electrode 30/wiring to connect the first N-region (col 9, lines 6-8; fig. 10)

forming electrode/wiring 244 connected to the P region (col 22, lines 38-40; fig. 39)

performing a cleaning step/processing step on the semiconductor substrate (col 20, lines 45-46), applying an etching solution/liquid to the semiconductor substrate to expose the wiring (col 20, lines 65-67, fig. 36), applying a He-Ne laser/light source on

the upper surface of the semiconductor substrate (col 21, lines 32-34), the He-Se laser having a wavelength of 600 nm (col 8, lines 54-55), which overlaps the claimed range of 500 nm to less than 1 microns

Miyawaki also discloses performing the cleaning step after polishing the semiconductor substrate (col 20, lines 40-46)

Since the method of Miyawaki uses the same steps, the same substrate and a light source having the same wavelength as that of the claimed invention, then under the principle of inherency using the light source in the method of Miyawaki would inherently reduce an electromotive force at a PN junction in said semiconductor substrate, thereby inhibiting galvanic effect due to photo excitation before, during or after the step including CMP, and preventing oxidation of a surface of said wiring.

Regarding claim 13, Miyawaki discloses forming a second N- region that is independent of the first N region (fig. 14)

Regarding claim 14, as seen in fig. 5 of Miyawaki, the total surface area of the N+/first N region and N-/second N region is smaller than the total surface of the P region, which encompasses the total surface area of the N+/first N region and N-/second N region is 100 to 1/100 times the total surface area of the P region

Regarding claim 15, as seen in fig. 10 of Miyawaki, the N- region/second N- region is formed extending to the periphery of the substrate

Regarding claim 16, Miyawaki discloses that the electrodes/wiring comprises of Al (col 9, lines 3-4)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki et al (US 5,952,694) in view of Klebanoff (US 6,169, 652)

Miyawaki's method has been described above. Unlike the instant claimed invention as per claim 3, Miyawaki fails to disclose that the processing/cleaning step is performed in a state in which the semiconductor substrate is grounded.

However, Klebanoff, in a method of using different chucks to hold semiconductor wafer during processing, teaches maintaining/controlling the semiconductor substrate at zero voltage (ground potential) during processing (col 3, lines 15-17)

Since both Miyawaki and Klebanoff are concerned with the step of cleaning the semiconductor substrate, one skilled in the art would have found it obvious to modify Miyawaki method by maintaining/controlling the semiconductor substrate at zero voltage (ground potential) during processing as per Klebanoff because Klebanoff states that employing a voltage-controlled electrostatic chuck will significantly reduce the likelihood of contaminant deposition on the substrate (see abstract)

Allowable Subject Matter

6. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 17, the cited prior art of record fails to disclose a method for manufacturing a semiconductor device wherein the exposing of the upper surface of the wiring of the semiconductor substrate to the liquid is performed concurrently with the exposing of the upper surface of the semiconductor substrate to the light source radiating light, in combination with the rest of the limitations of claim 17

Response to Arguments

7. Applicant's arguments filed 12/16/2004 have been fully considered but they are not persuasive.

Applicants argue that there is no connection between p+ region and n+ region in Miyawaki, as required in claim 1. This argument is unpersuasive because while it is true that there is no connection between p+ region 12 and n+ region 14 in Miyawaki, it is also true that fig. 10 of Miyawaki shows a wiring 30 connected to a n+ region 14/first N region, which meets the requirement of claim 1 since claim 1 recites "forming wiring so as to connect one or both of the first N and the P regions". The applicants also argue that fig. 10 of Miyawaki does not disclose forming a first N-region and a P region on a

substrate. This argument is unpersuasive because as clearly shown in fig. 10 of Miyawaki, a first N-region and a P region are formed on a substrate.

Applicants argue that there is no indication that Miyawaki discloses or suggest performing a processing step on a semiconductor substrate on which the upper surface of said wiring is exposed using a liquid applied to said semiconductor substrate and a light source radiating light onto said semiconductor substrate because there is no citation to a processing step that exposes wiring and that includes exposure to liquid and exposure to a light, as recited in claim 1. This argument is unpersuasive because the claim language of "performing a processing step on a semiconductor substrate on which the upper surface of said wiring is exposed using a liquid applied to said semiconductor substrate and a light source radiating light onto said semiconductor substrate" does not necessarily require that the upper surface of the wiring is exposed by using processing step that includes exposure to liquid and exposure to a light. The above mention claim language can be interpreted as the upper surface of said wiring is already exposed before the steps of using a liquid applied to said semiconductor substrate and a light source radiating light onto said semiconductor

It is argued that Miyawaki is not concerned with the step of cleaning the semiconductor substrate because Miyawaki discloses " a monocrystalline Si body 1' having the oxide film 4 is cleaned". This argument is unpersuasive because fig. 32 of Miyawaki shows semiconductor layer 1 is formed on " a monocrystalline Si body 1' having the oxide film 4', which implies that the monocrystalline Si body 1' having the

oxide film 4 function as a semiconductor substrate. Thus, the examiner asserts that Miyawaki is concerned with the step of cleaning the semiconductor substrate

Applicants argue that Miyawaki does not teach that the wire is connected to the P region as required in claim 18. The examiner disagrees because as shown in fig. 39 of Miyawaki, the wiring 244 is connected to the P region.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
June 24, 2005